REMARKS

By the present response, Applicant has amended claim 8 to further clarify the invention. Claims 1-23 are pending in this application. Reconsideration and withdrawal of the outstanding rejections and allowance of the present application are respectfully requested in view of the above amendments and the following remarks.

In the Office Action, claim 8 has been objected to because of informalities. Claims 1-23 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,802,015 (Atkinson).

Claim Objections

Claim 8 has been objected to because of informalities. Applicant has amended this claim to further clarify the invention and respectfully requests that this objection be withdrawn.

35 U.S.C. § 102 Rejections

Claims 1-23 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Atkinson. Applicant respectfully traverses these rejections.

Atkinson discloses a computer system that supports operation of a CPU at multiple clutch speeds where logic in the computer system predicts the performance requirements of the CPU, and selects the fastest clock speed to optimize performance. A keyboard controller receives user inputs from various user input devices, including a mouse and keyboard. The keyboard controller identifies user inputs that reflect a system command, such as a mouse click,

selection of the ALT. key with another key, or any special function keys associated with a software application. If such a user input is detected, the keyboard controller generates a system management interrupt to the CPU. In response, the CPU calls a speed control algorithm that identifies the source of the SMI and increases the clock speed to the processor.

Regarding claims 1, 8, 15 and 21, Applicant submits that Atkinson does not disclose or suggest the limitations in the combination of each of these claims. For example, the Examiner asserts that Atkinson discloses determining whether a bus master device is in an active state when the SMI signal is for performing CPU speed transition, by the PCI bus 124 in Fig. 1 and col. 7, lines 58-62. However, a PCI bus, that interconnects devices, is not a bus master device, as recited in the claims of the present application. A PCI bus as disclosed in Atkinson is merely a set of interconnections, e.g., wires that interconnect devices.

Further, the cited portions in col. 7 of Atkinson merely discloses that the keyboard controller transmits a system management interrupt (SMI) to a speed control algorithm preferable stored in the BIOS ROM that executes on the CPU or on another programmable device in the computer system. This is not determining whether a bus master device is in an active state when the SMI signal is for performing CPU speed transition. The cited portions of Atkinson do not disclose or suggest a bus master device being in an active state. Further, there is no disclosure or suggestion of a bus master being in an active state when the SMI signal is for performing CPU speed transition, as recited in the claims of the present application.

Further, the Examiner asserts that Atkinson discloses canceling the CPU speed transition operation when the bus master device is in the active state and generating at prescribed intervals a retry SMI signal, at col. 9, lines 5-7. However, these portions merely disclose that the keyboard controller will assert its SMI source to the CPU if the "make code" is listed in the system command identification table in the keyboard controller or if a mouse button has been double-clicked, and that conversely, if the make code represents another key is pressed, or if the mouse packet indicated x/y movement, or a single button press, then no SMI will be generated and the CPU will stay in its most efficient power mode state. This is not canceling a CPU speed transition operation when the bus master device is in the active state and generating at prescribed intervals a retry SMI signal, as recited in the claims of the present application. As noted previously, Atkinson does not disclose or suggest a bus master device, or a bus master device being in an active state. Further, Atkinson does not disclose or suggest a retry SMI signal or generating at prescribed intervals a retry SMI signal. Atkinson merely relates to a keyboard controller asserting its SMI source to the CPU based on a make code being listed in a table or mouse buttons being depressed or a mouse being moved.

Moreover, the Examiner asserts that Atkinson discloses active state checking means for checking an active state of a predetermined device, by the real time clock, PCI bus 124 and col. 7, line 32. However, as noted previously, a PCI bus is not a device. Further, Atkinson merely discloses that the keyboard controller typically incorporates a counter or a real time clock to

track the acitivities of certain components such as the hard drive and the PCI bus and may induce a sleep mode or reduced power mode after a predetermined time of inactivity. This is not an active state checking means for checking an active state of a predetermined device, as recited in the claims of the present application. Atkinson merely discloses that a counter or a real time clock is used to determine that a predetermined time has elapsed whereby the keyboard controller may then induce a sleep mode or reduced power mode. A real time clock is merely a clock that usually runs even when the computer is off and that is used to keep track of the time and date even when the computer is turned off. A real time clock, as is well understood by one of ordinary skill in the art, is not an active state checking means for checking an active state of a predetermined device.

The Examiner further asserts that Atkinson discloses an interrupt generating means for creating a second interrupt signal to retry the prescribed operation for the CPU speed transition when the interrupt occurrence reason recognition means determines that a first interrupt signal is created for the CPU speed transition and the active state checking means determines that the predetermined device is in the active state, by the south bridge 168 in Fig. 1. However, Atkinson merely discloses that south bridge 68 couples or bridges the primary expansion bus 124 to other secondary expansion buses (see col. 6, lines 47-49), and that the south bridge may generate a stop clock interrupt to the CPU requesting the CPU to stop operation based on a particular system event, or based on a user command (see col. 6, lines 62-65). The south bridge disclosed

in Atkinson is not an interrupt generating means for creating a second interrupt signal to retry the prescribed operation for the CPU speed transition when the interrupt occurrence reason recognition means determines that a first interrupt signal is created for the CPU speed transition and the active state checking means determines that the predetermined device is in the active state, as recited in the claims of the present application. Then south bridge generating an interrupt to the CPU based on a particular system event or a user command does not disclose or suggest these limitations as recited in the claims of the present application. The interrupt generated by the south bridge is not a second interrupt signal to retry the prescribed operation for the CPU speed transition, as recited in the claims of the present application.

Regarding claims 2-7, 9-14, 16-20, 22 and 23, Applicant submits that these claims are dependent on one of independent claims 1, 8, 15 and 21 and, therefore, are patentable at least for the same reasons noted previously regarding these independent claims.

Accordingly, Applicants submit that Atkinson does not disclose or suggest the limitations in the combination of each of claims 1-23 of the present application. Applicant respectfully requests that these rejections be withdrawn and that these claims be allowed.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant submits that claims 1-23 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, Frederick D. Bailey, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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